IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Wendell P. Noble et al.	Examiner: Michael Trinh	
Serial No.:	09/551,027	Group Art Unit: 2822	
Filed:	April 17, 2000	Docket: 303.379US2	
Title:	CIRCUIT AND METHOD FOR A FOLDED BIT LINE MEMORY CELL WITH VERTICAL TRANSISTOR AND TRENCH CAPACITOR		

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
Washington, D.C. 20231

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Supplemental Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Pursuant to 37 C.F.R. §1.97(c)(2), please charge the fee of $180.00 as set forth in 37 C.F.R. §1.17(p) to Deposit Account No. 19-0743.

The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

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Respectfully submitted,

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By their Representatives,

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Date 12-23-02 By _____

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 23 day of December, 2002.

Tina Kohout
Name

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Signature